

## **Michael L. Lewis**

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### *Work*

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## **Objective**

Senior-level ASIC/SoC design position which allows me to use and continue to develop my breadth of abilities in digital design activities, including architecture, specification, HDL implementation, verification, synthesis, static timing analysis, and design-for-test.

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## **Skills**

Programming & Scripting Languages... Verilog, VHDL, SystemC, Perl, Tcl, 8051 Assembly, Sed

Electronic Design Automation ..... Synopsys (Design Compiler, Physical Compiler, PrimeTime, DFT Compiler, TetraMax)  
Cadence (Verilog-XL, NC-Sim, SimVision, LEC, Opus)  
Mentor Graphics ModelSim  
Atrenta SpyGlass  
SynTest TurboFault  
Xilinx Foundation

Standards & Competencies..... USB 1.1, USB 2.0, AMBA, IEEE Std. 1149.1 (JTAG), 8051

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## **Experience**

### **1999-Present—Cypress Semiconductor, Personal Communications Division – San Diego, CA/Boise, ID**

- 1) West Bridge(TM) Second Generation Mobile Peripheral: Owned global control block responsible for all clocks, resets, test control, power control, and IO control on million-gate ASIC; Created verilog models of all interfaces, and devised tool to automatically generate IO interface; Managed top-level integration and enhanced RTL release methodology
- 2) Programmable System on Chip (PSoC): Contained significant problems in test quality by creating functional vectors to improve digital fault coverage using SynTest's TurboFault on six devices, led team of engineers and liaised with management by providing project schedule and status metrics, delivered vectors two quarters ahead of original schedule by automating low-level vector development using perl. Also created system-level model for verification environment using SystemC for next generation PSoC family of products.
- 3) West Bridge(TM) Ultra-Low-Power Mobile Peripheral: Owned majority of digital logic of a 500 Kgate ASIC; interfaced with key customer in defining design requirements; guided efforts of project from feasibility, architecture, and design of highly-constrained (area, power, and time-to-market) product; assisted verification engineers towards design closure; worked with firmware engineers during application development; and interfaced with physical designers to solve significant barriers to timing closure. Devised productivity initiatives which saved several man-weeks of effort on synthesis quality and timing closure ECOs.
- 4) Low-Power Wireless Peripheral Transceiver: Implemented digital components of a proprietary wireless interface using Synopsys Design Compiler, Power Compiler, and DFT Compiler; worked with design engineers on DFT enhancements; generated and verified

ATPG vectors with Synopsys TetraMax; closed timing using Synopsys PrimeTime; and interfaced with back-end engineers on design closure;

- 5) USB 2.0 Low-Power Mobile Microcontroller Peripheral: Mentored and supported international team of system engineers, designers, and marketers on a project enabling a low-power interface for embedding high-speed USB on cell phone and other mobile devices.
- 6) USB 2.0 Low-Power Integrated Microcontroller Peripheral: Worked from start-to-finish on project feasibility, project scheduling, configuration management, defect management, architecture, block-level RTL design and verification, padding generation using perl, IP preparation, top-level integration, design analysis using Spyglass, formal equivalency checking, static timing analysis with Synopsys PrimeTime, back-end liason, and post-silicon test, characterization, and validation support for a low-power, 0.15 $\mu$ m ASSP. Led team of design, test, product, and technology engineers, involved in standard cell library accuracy improvements, and compared silicon results to characterized library to unravel standard cell characterization inaccuracies.
- 7) USB 2.0 Macrocell Transceiver Interface ASIC: Technical lead responsibilities included RTL design, DFT, verification, documentation, IP preparation, and back-end liason. Achieved first-pass functional success.
- 8) USB 2.0 Integrated Microcontroller Peripheral: RTL design (IP used on four projects,) full-system functional verification and regression using Verilog and 8051 assembly, Synopsys library model generation, design-for-test, scan vector generation, documentation, and post-silicon test, characterization, and validation support. Two patents filed.
- 9) USB 2.0 Bus Functional Models (Host and Monitor): Behavioral Verilog design, verification, testbench enhancements (including packet/transaction-based tasks, and text I/O processing,) documentation, and corporate-wide integration (used on four projects to date.)
- 10) USB 1.1 Cost-Reduction ASIC: Full-system functional verification and regression, scan vector generation, test engineering liason.
- 11) USB 1.1 IP Transfer: Successful completion of a \$2 million dollar contract by providing customer with IP-quality database, documentation, on-site training, design, and verification assistance.
- 12) Bluetooth Integrated Microcontroller: USB-side functional verification, testbench generation, and documentation.
- 13) Corporate Initiatives: Provided design expertise to corporate CAD engineers on support of Synopsys' PrimeTime-SI and Tetramax design tools; supplied design productivity scripts in perl and tcl to corporate tool repository; worked on corporate task-force to improve DFT best practices and provide DFT-improvement guidance on existing products; supported corporate design community in use of Synopsys tools, training, and technical conferences; provided corporate presence as a member of the Synopsys Users' Group (SNUG) technical committee; and mentored junior engineers in design and verification tools and languages

#### **1997-1999—TRW, Avionics Systems Division – San Diego, CA.**

- 1) Multi-bus Interface ASIC: VHDL RTL design, testbench generation, functional verification, and documentation of an interface ASIC used in the communication, identification, and navigation subsystem of the Air Force F-22 fighter jet platform.
- 2) Low-latency Signal Processing Module: HW/SW integration and test, die-level hardware work-arounds with focused ion beam technology, avoided costly ASIC re-spins, schedule delays, and late customer deliveries. Designed for the F-22 platform.
- 3) High-speed Parallel-to-Serial Bus Interface FPGAs (Master, Slave, and Monitor): VHDL RTL design, testbench generation, functional verification, synthesis, place and route, timing analysis, and documentation of an avionics bus used in the communication, identification, and navigation subsystem of the Joint Strike Fighter (JSF) platform.

### **1996—Rockwell Network Systems – Santa Barbara, CA**

Contracted in the design process of a PCI-FDDI interface ASIC for a network interface card. Tasks included VHDL design, simulation, verification, and documentation.

### **1994—Digital Prototype Systems – Fresno, CA**

Performed quality assurance, product testing, RMAs, manufacturing, field applications, and customer technical support for telemetry monitoring engineering firm.

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## **Education**

California State University, Fresno – Department of Electrical Engineering  
BSEE (Magna Cum Laude), December 1994

University of California, Santa Barbara – Department of Electrical and Computer Engineering  
MSEE, December 1996

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## **Publications & Industry Work**

“Adopting Software Methods for VHDL Design,”  
*Integrated Systems Design*, October 1999.

“Testing a Super-Fast Part on a Super-Cheap Tester,”  
*Cypress International Technical Conference*, June 2000.

“Tricks of the Test Trade: ATPG Methods that Improve Fault Coverage of SoC Devices,”  
*Synopsys User’s Group (SNUG)*, March 2002 (3<sup>rd</sup> Place, Best Paper Award).  
*Cypress International Technical Conference*, July 2002.

“DFT Considerations in Scan Design to Enable Vector Partitioning,”  
*IEEE International Workshop on Test Resource Partitioning (TRP)*, October 2002

“Attributes for Dummies... or Getting Under the Hood of Synopsys,”  
*Cypress Logic Excellence Summit*, February 2008

“Synopsys Clock Constraints Generation Tool,”  
*Cypress Logic Excellence Summit*, February 2008

175 Cypress Internal Memos and Specifications

Synopsys Users’ Group (SNUG) Technical Committee Member, 2006-2007

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## **Patents**

6,857,088: “Method and system for testing the logic of a complex digital circuit containing embedded memory arrays”, issued February 15, 2005

6,959,257: “Apparatus and method to test high speed devices with a low speed tester”, issued October 25, 2005

Pending: “Devices and methods for sharing common target device with two different hosts according to common communication protocol,” filed September 2007